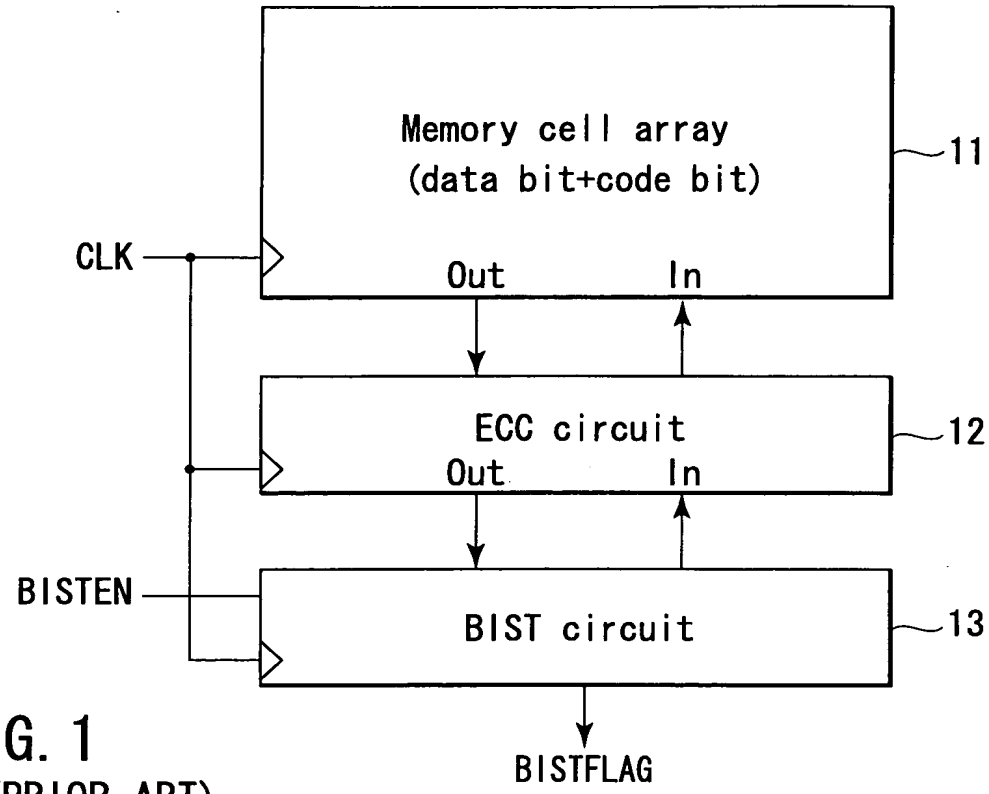
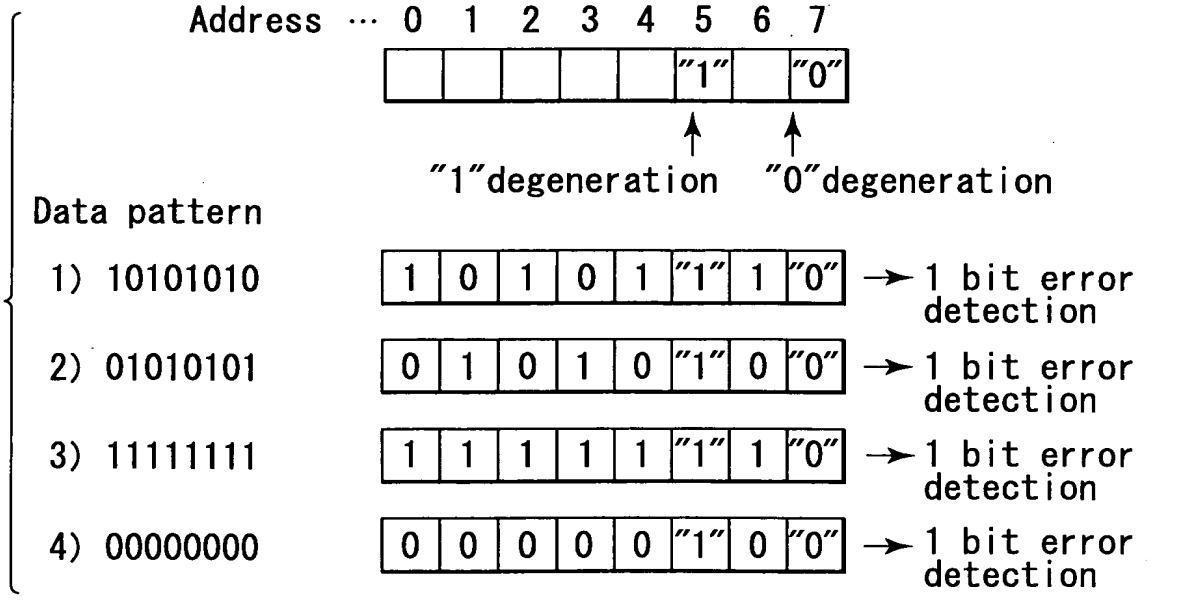


FIG. 1
(PRIOR ART)



※ Two bits of addresses 5, 7 are defective, but a product is processed as nondefective

FIG. 2 (PRIOR ART)

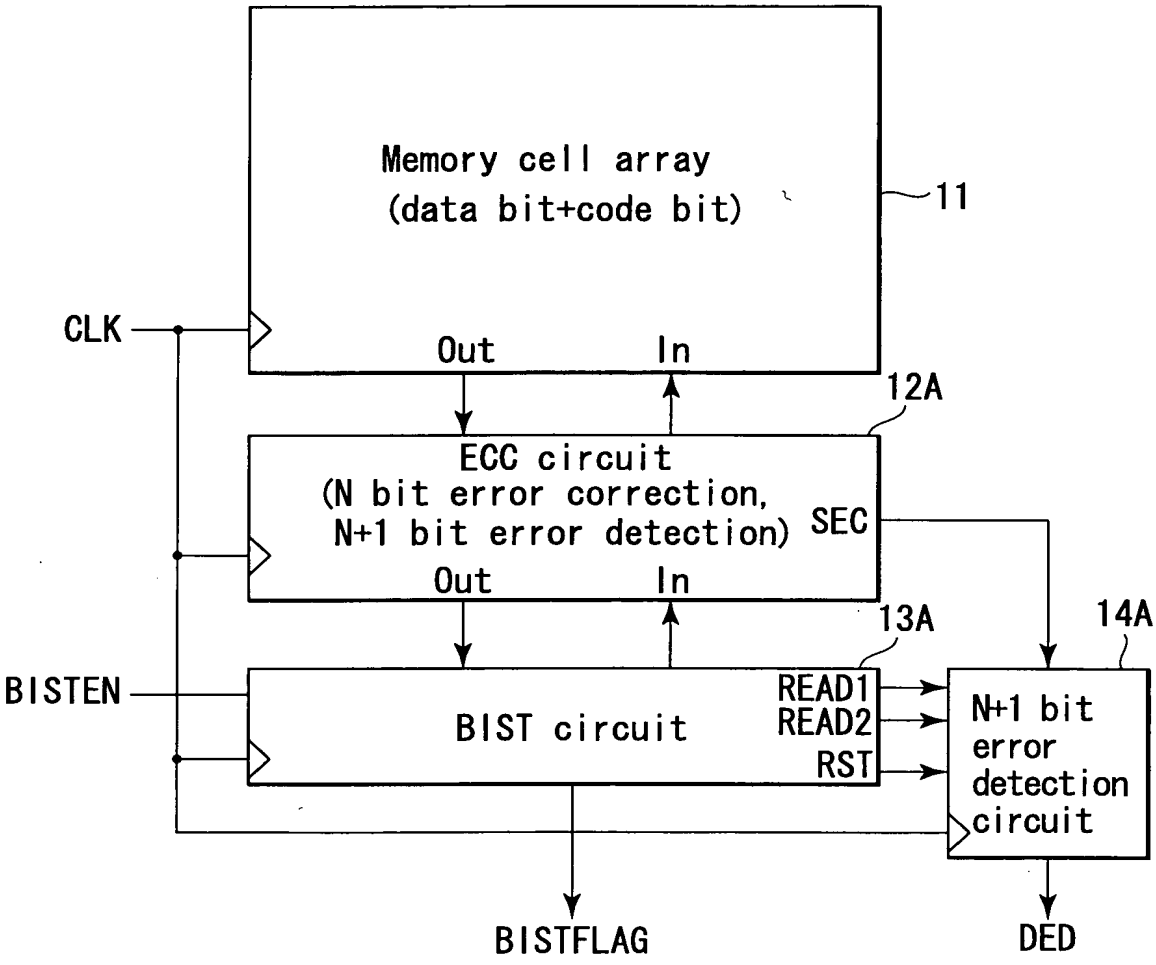

Memory cell array
(data bit+code bit)
11
CLK
Out
In
12A
ECC circuit
(N bit error correction,
N+1 bit error detection)
SEC
Out
In
13A
14A
BISTEN
BIST circuit
READ1
READ2
RST
N+1 bit
error
detection
circuit
BISTFLAG
DED

FIG. 3

Test method 1(in the case of memory on which ECC circuit capable of N bit error correction, N+1 bit error detection is mounted)

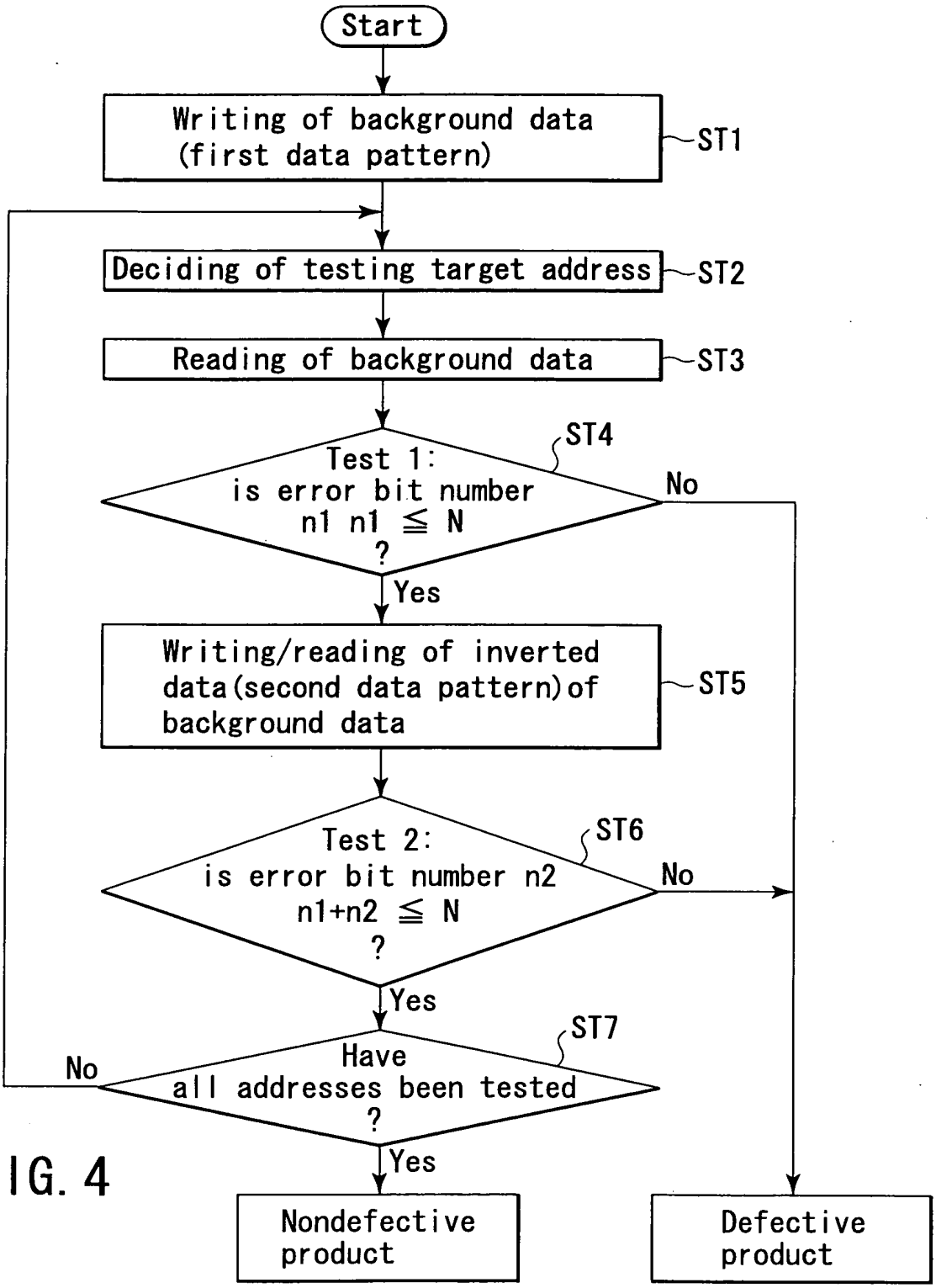


FIG. 4

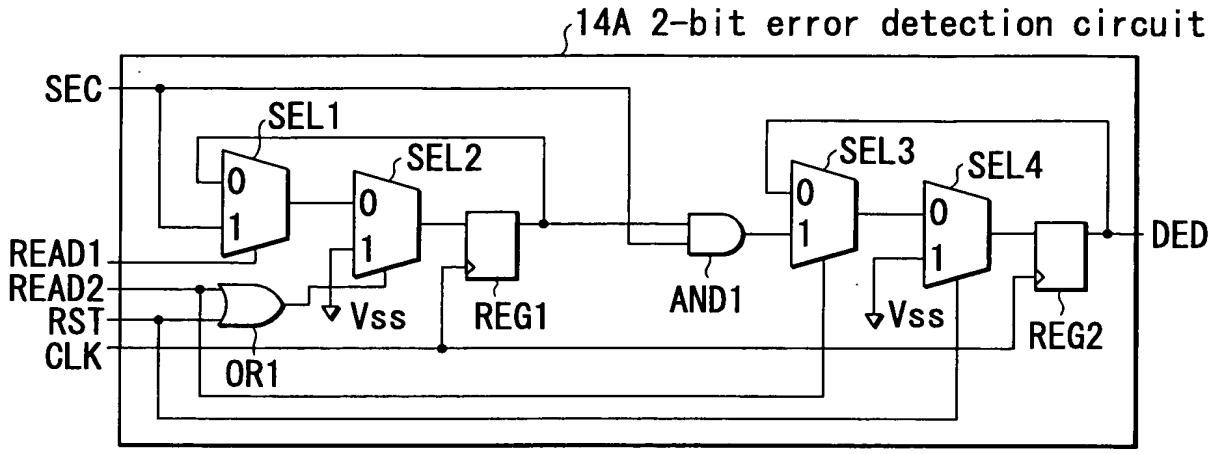

14A 2-bit error detection circuit
SEC
SEL1
SEL2
SEL3
SEL4
READ1
READ2
RST
CLK
OR1
Vss
REG1
AND1
Vss
REG2
DED

FIG. 5

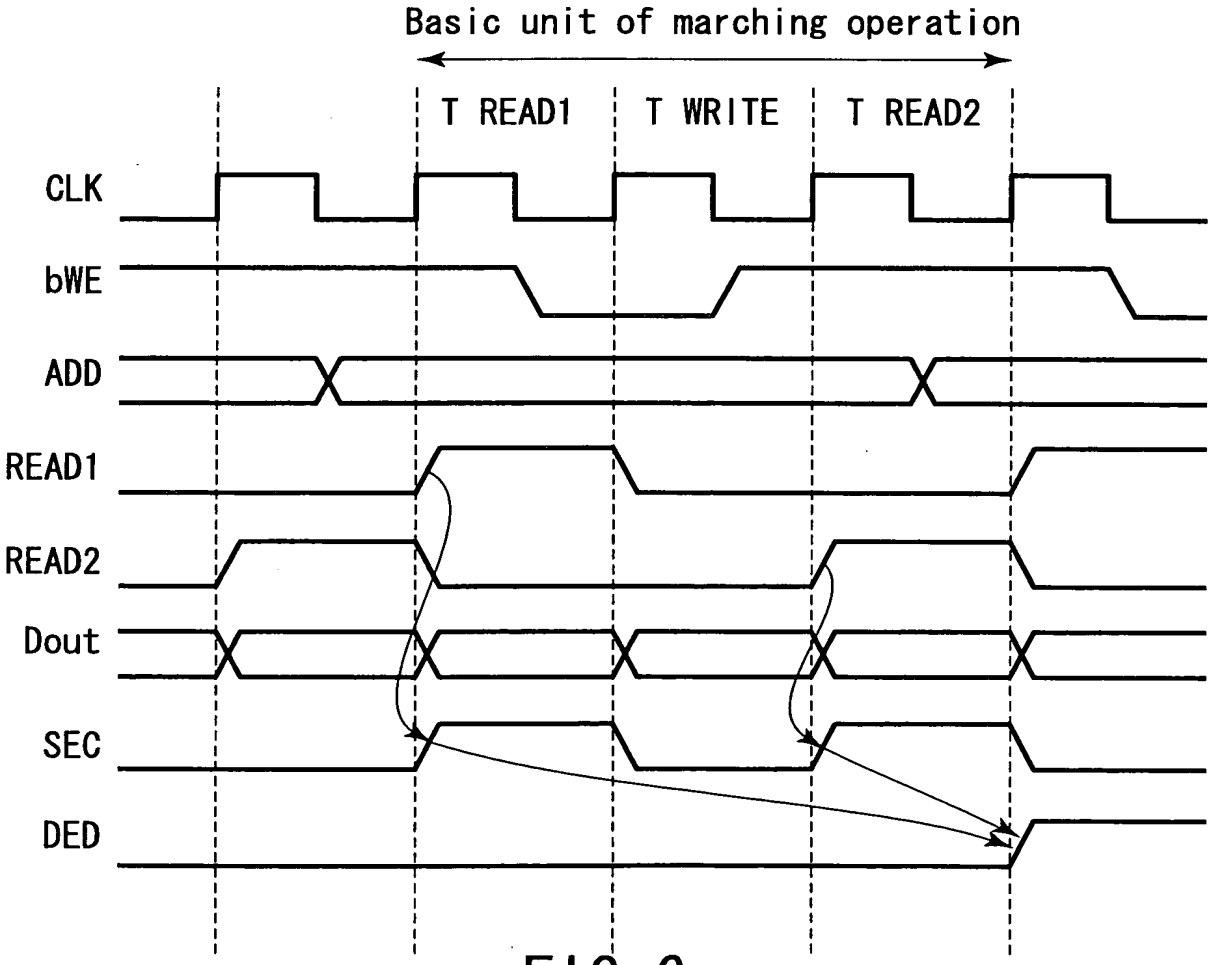
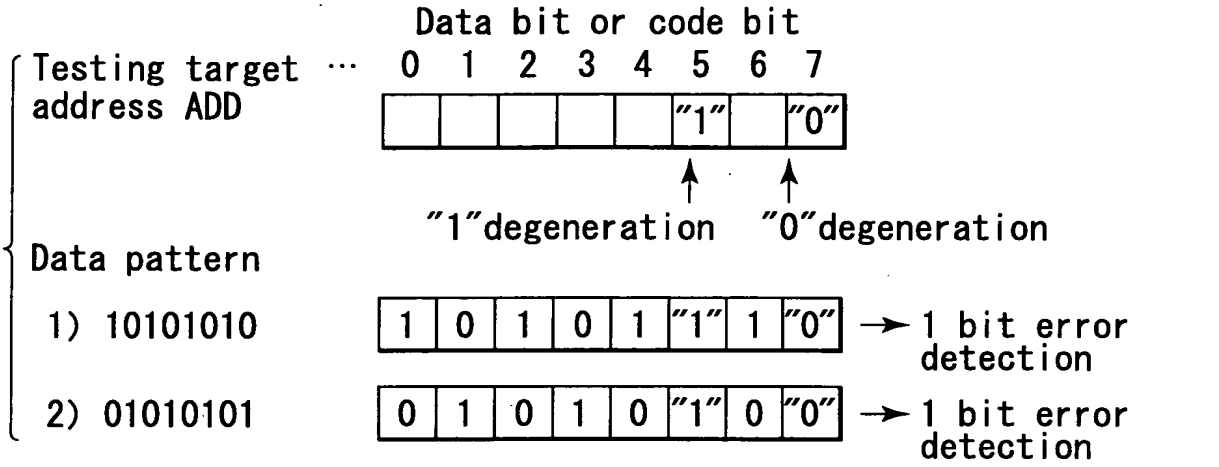

Basic unit of marching operation
T READ1
T WRITE
T READ2
CLK
bWE
ADD
READ1
READ2
Dout
SEC
DED

FIG. 6



※ Since two bits of addresses 5, 7 are defective, a product is processed as defective

FIG. 7

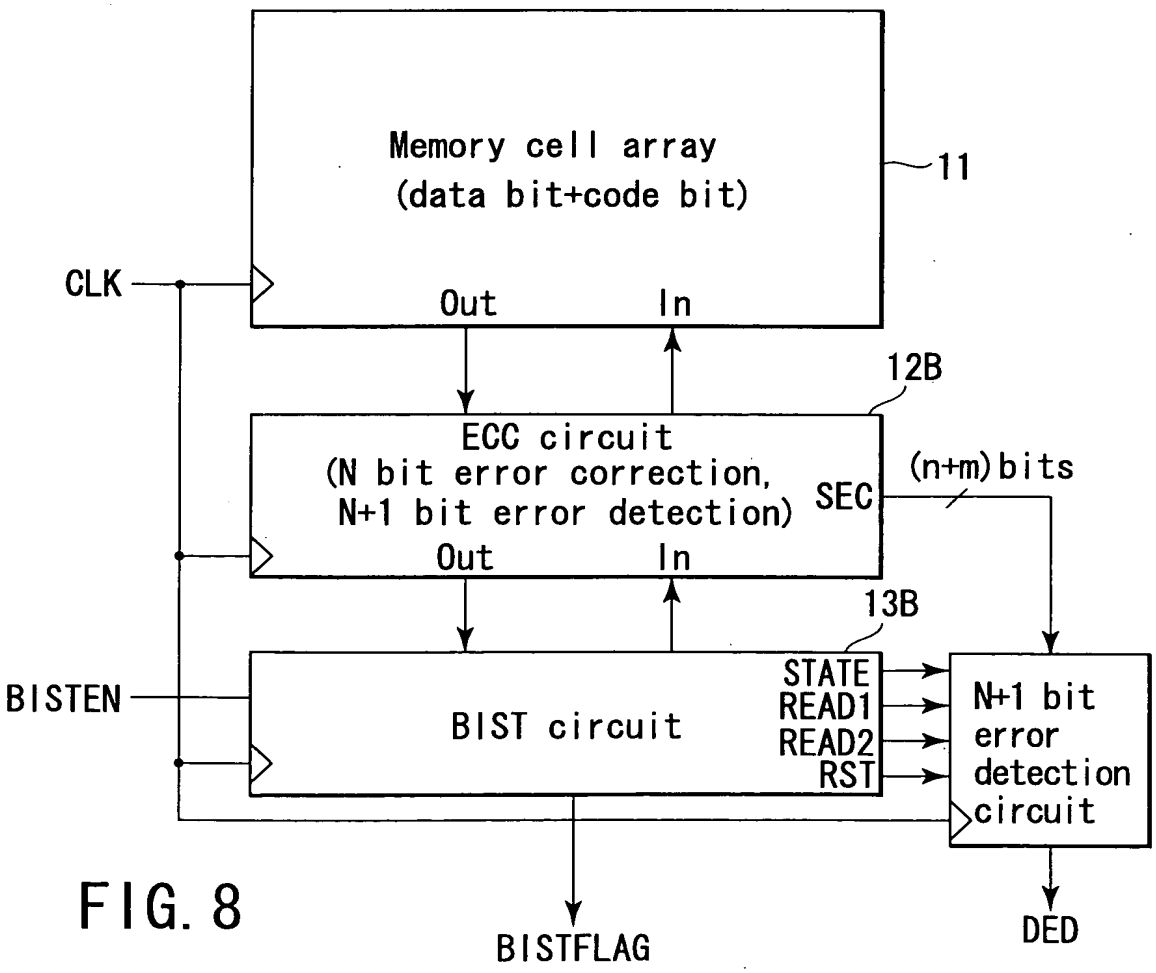


FIG. 8

Test method 2(in the case of memory on which ECC circuit capable of N bit error correction, N+1 bit error detection is mounted)

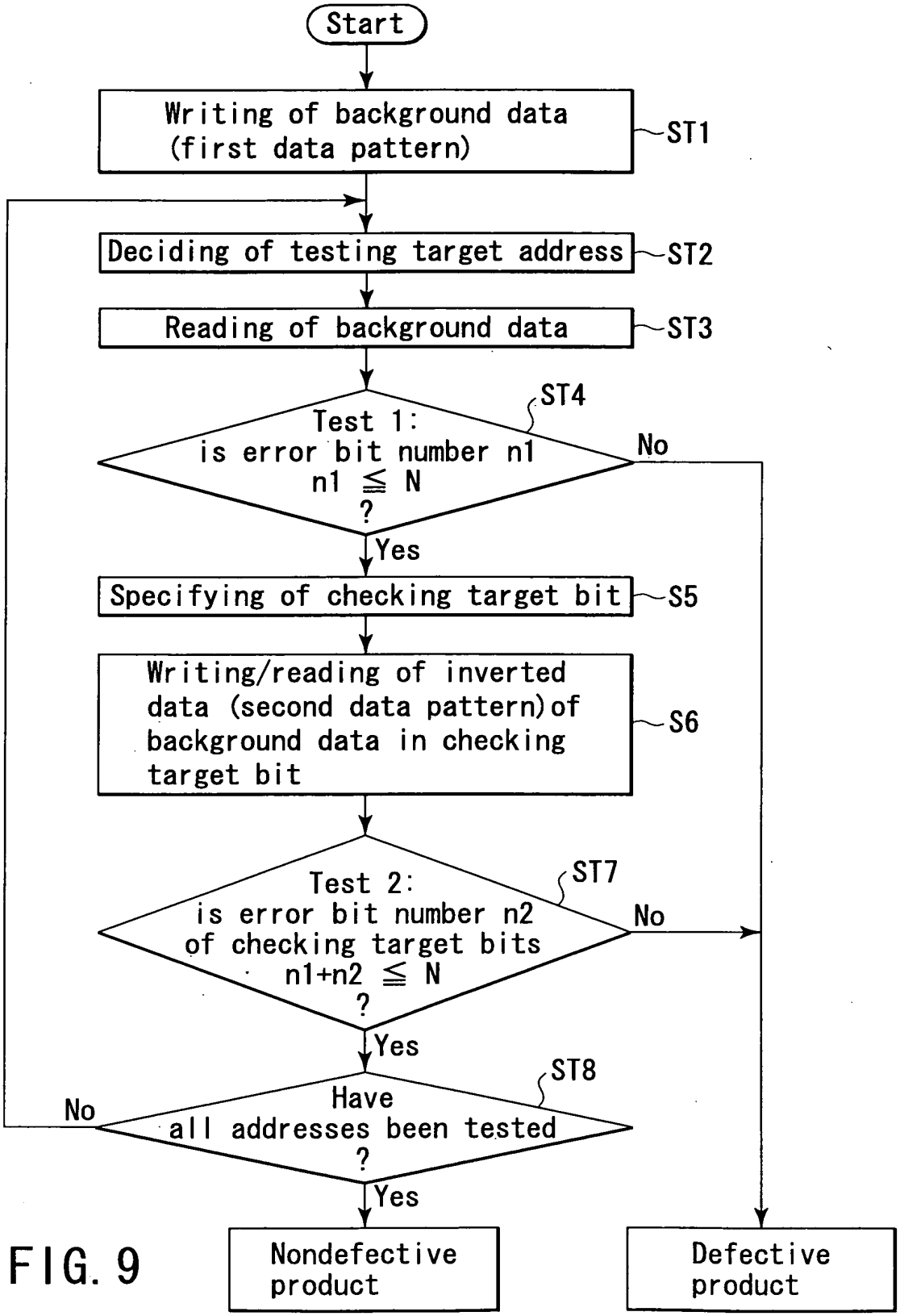


FIG. 9

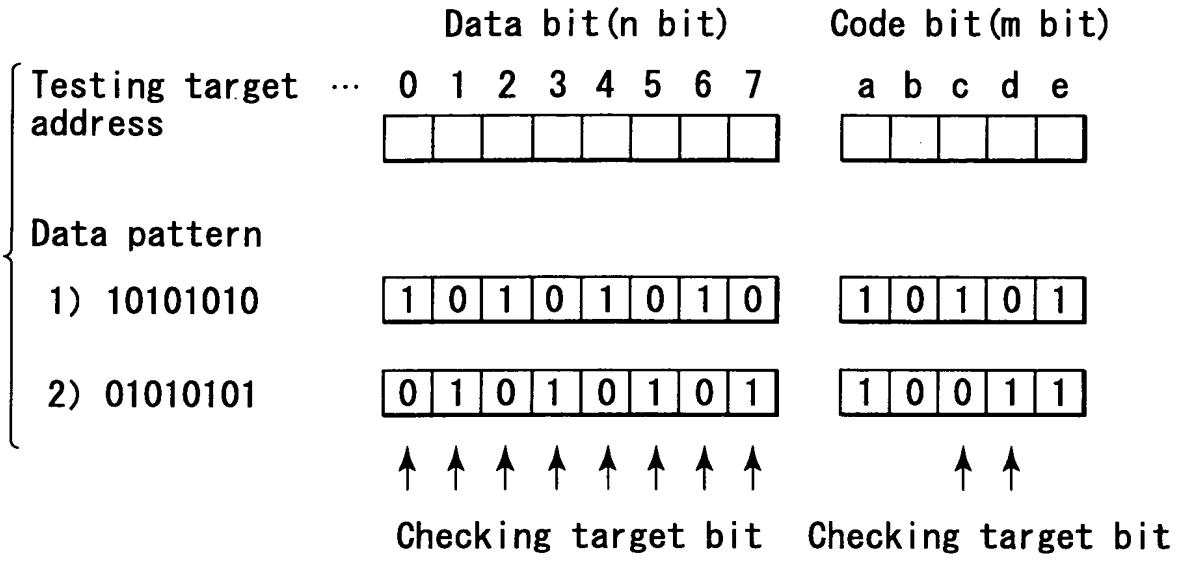

Data bit(n bit)
Code bit(m bit)
Testing target address
0 1 2 3 4 5 6 7
a b c d e
Data pattern
1) 10101010
1 0 1 0 1 0 1 0
1 0 1 0 1
2) 01010101
0 1 0 1 0 1 0 1
1 0 0 1 1
Checking target bit
Checking target bit
※ In test 2, addresses a, b, e are not checked

FIG. 10

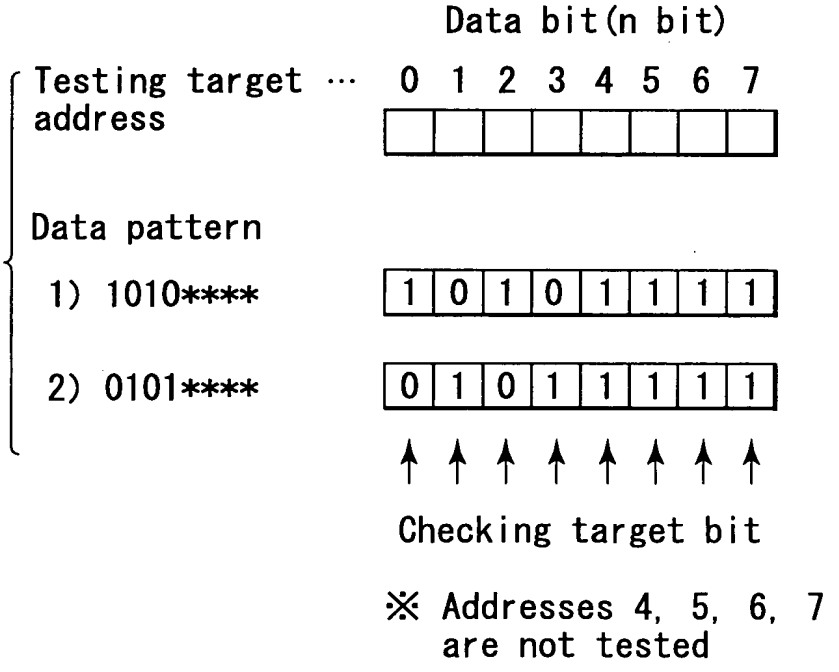

Data bit(n bit)
Testing target address
0 1 2 3 4 5 6 7
Data pattern
1) 1010****
1 0 1 0 1 1 1 1
2) 0101****
0 1 0 1 1 1 1 1
Checking target bit
※ Addresses 4, 5, 6, 7 are not tested

FIG. 11

FIG. 12

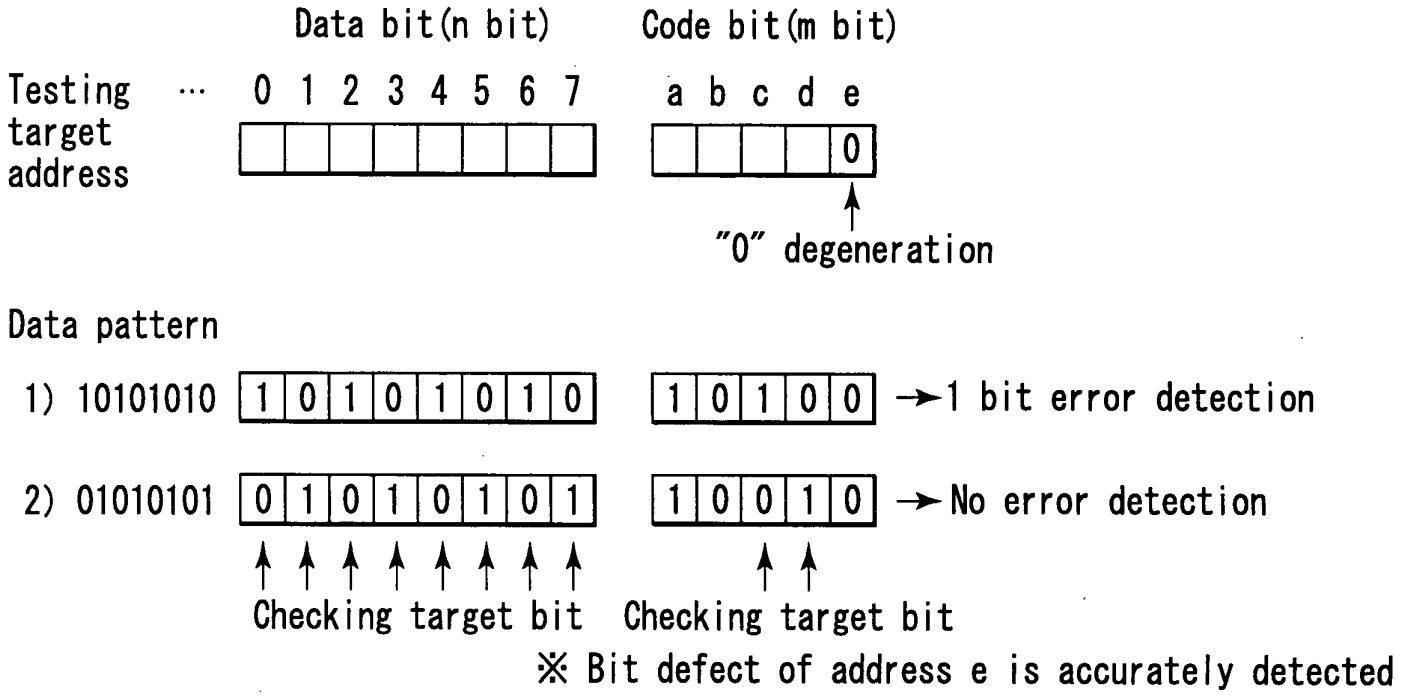


FIG. 13